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PATENT APPLICATION

ATTORNEY DOCKET NO. 200310842-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	**Peter J. Fricke et al.**	**Confirmation No.:**	**5316**
Application No.:	**10/772,945**	**Examiner:**	**NADAV, Ori**
Filing Date:	**February 4, 2004**	**Group Art Unit:**	**2811**

Title: Memory Array with Two-Terminal Crosspoints Using Silicon-Rich Insulator

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on January 20, 2009 .

☒ The fee for filing this Appeal Brief is $540.00 (37 CFR 41.20). - minus $510.00 per previously filed Appeal Brief dated July 30, 2008.

☐ No Additional Fee Required.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☐ 1st Month $130	☐ 2nd Month $490	☐ 3rd Month $1110	☐ 4th Month $1730

☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 30 . At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees.

Respectfully submitted,

Peter J. Fricke et al.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the Patent Application of

Peter J. Fricke et al.

Application No. 10/772,945

Filed: February 4, 2004

For: Memory Array with Two-Terminal Crosspoints Using Silicon-Rich Insulator (as amended)

Group Art Unit: 2811

Examiner: NADAV, Ori

Confirmation No.: 5316

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
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P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to Appellants' filing of an Appeal Brief on 30 July 2008, the Examiner of this application reopened prosecution with a final Office Action dated 21 October 2008 (the "Office Action" or the "Action"). Appellant wishes to note that it is improper for this Action to have been made final since the new grounds of rejection made were not necessitated by Appellant having amended any claims. Appellant had previously filed an Appeal Brief and *not* an amendment to any claim.

Nevertheless, having reviewed the new grounds of rejection raised in the Office Action of 21 October, Appellants hereby request re-instatement of the appeal in this application and files the present, updated Appeal Brief, along with a new Notice of Appeal, in support of the re-instated appeal.

I. Real Party in Interest

The real party in interest is Hewlett-Packard Development Company, LP, a limited partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

II. Related Appeals and Interferences

There are no appeals or interferences related to the present application of which the Appellant is aware.

III. Status of Claims

Claims 7, 34 and 35 have been previously cancelled without prejudice or disclaimer.

Claims 2, 12-15, 17-25, 36, 37, 42-46 and 50-54 have been withdrawn from consideration but remain at issue because they are subject to rejoinder upon the allowance of a pending independent claim.

Claims 1, 3-6, 8-11, 16, 26-33, 38-41, 47-49 and 55-59 are pending in the application and stand finally rejected.

Accordingly, Appellant appeals from the final rejection of claims 1, 3-6, 8-11, 16, 26-33, 38-41, 47-49 and 55-59, which claims are presented in the Appendix.

IV. Status of Amendments

No amendments have been filed subsequent to the final Office Action of October 21, 2008, from which Appellant takes this appeal.

V. Summary of Claimed Subject Matter

The present application discloses a memory array comprising a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points. (*Appellants' specification, Abstract*). A memory cell is disposed at each cross-point, each memory cell having a storage element and a control element coupled in series between a row conductor and a column conductor, and each control element including a silicon-rich insulator. (*Appellants' specification, Abstract*).

The layer (60) of silicon-rich insulator, for example a silicon-rich oxide (SRO), of the control element (45) provides for enhanced current injection into the dielectric of a tunnel junction layer (70). (*Appellants' specification, paragraph 0034*). Other advantages include improved isolation of each memory cell within the memory array thus resulting in significant reduction of cumulative sneak-path currents. (*Appellants' specification, paragraph 0035*). Still other advantages may include increased size of sub-arrays, lower manufacturing costs, ease of manufacturing without incurring destruction to other elements, increased compatibility with other devices, ability to produce devices having dimensions below 0.5 micrometers, and the silicon-rich insulator's ability to act like a control element due to its asymmetric rectification characteristics. (*Appellants' specification, paragraphs 0034-0036*).

Turning to Appellant's specific claims,

Claim 1 recites:

A memory array (10) comprising:

a) a multiplicity of row conductors (30) and a multiplicity of column conductors (40), the row conductors (30) and column conductors (40) being arranged to cross at cross-points, (*Appellants' specification, paragraphs 0028, 0033 and, 0062*) and

b) a memory cell (20) disposed at each cross-point, each memory cell (20) having exactly two terminals (*Appellants' specification, paragraphs 0039, 0051, and 0052, and Figs. 3, 14, and 15*) and having a storage element (50) and a control element (45) coupled in series between a row conductor (30) and a column conductor (40), each control element (45) including a tunnel junction (70) and a silicon-rich insulator (60) (*Appellants' specification, paragraphs 0031 and 0033*), wherein the silicon-rich insulator (60) injects current into the tunnel junction (70) when the memory cell (20) is selected (*Appellants' specification, paragraph 0034*).

Claim 16 recites:

A memory array (10) comprising:

a) a multiplicity of row conductors (30) and a multiplicity of column conductors (40), the row conductors (30) and column conductors (40) being arranged to cross at cross-points (*Appellants' specification, paragraphs 0028, 0033 and, 0062*), and

b) a memory cell (20) disposed at each cross-point, each memory cell (20) having exactly two terminals (*Appellants' specification, paragraphs 0039, 0051, and 0052, and Figs. 3, 14, and 15*), each memory cell (20) comprising means for storing data (50) and means for controlling (45) the means for storing data, the means for storing data (50) and means for controlling (45) being coupled in series between a row conductor (30) and a column conductor (40), each means for controlling (45) including a tunnel junction (70) and a silicon-rich insulator (60) (*Appellants' specification, paragraphs 0031 and 0033*), wherein the silicon-rich insulator (60) injects current into the tunnel junction (70) when the memory cell (20) is selected (*Appellants' specification, paragraph 0034*).

Claim 26 recites:

A memory cell (20) made by a method comprising:

a) providing a substrate (300) (Step 10) (*Appellants' specification, paragraph 0055, and Fig. 16*),

b) depositing and patterning a first conductive layer (30 or 40) over the substrate (300) (Steps 20 and 30) (*Appellants' specification, paragraph 0056, and Fig. 16*),

c) forming a storage layer (50) over the patterned first conductive layer (30 or 40) (Step 40) (*Appellants' specification, paragraph 0056, and Fig. 16*),

d) forming a layer of silicon-rich insulator (60) over the storage layer (50) (Step 50) (*Appellants' specification, paragraph 0056, and Fig. 16*),

e) forming a tunnel-junction layer (70) over the layer of silicon-rich insulator (60) (Step 60) (*Appellants' specification, paragraph 0056, and Fig. 16*), and

f) forming and patterning a second conductive layer (40 or 30) over the tunnel-junction layer (70) (Steps 70 and 80) (*Appellants' specification, paragraph 0056, and Fig. 16*), whereby a memory-cell stack is formed, the stack having a storage layer (50), a silicon-rich insulator (60), and a tunnel-junction layer (70) in series relationship between the first and second conductive layers (30 and 40) (*Appellants' specification, paragraphs 0055 and 0056*), whereby the first and second conductive layers (30 and 40) are adapted to provide exactly two terminals for control of the memory cell (20) (*Appellants' specification, paragraphs 0039, 0051, and 0052, and Figs. 3, 14, and 15*), wherein the silicon-rich insulator (60) injects current into the tunnel-junction layer (70) when the memory cell (20) is selected (*Appellants' specification, paragraph 0034*).

Claim 38 recites:

A memory cell (20) made by a method comprising:

a) providing a substrate (300) (Step 10) (*Appellants' specification, paragraph 0055, and Fig. 16*),

b) depositing and patterning a first conductive layer (30 or 40) over the substrate (300) (Steps 20 and 30) (*Appellants' specification, paragraph 0056, and Fig. 16*),

c) forming a storage layer (50) over the patterned first conductive layer (30 or 40) (Step 40) (*Appellants' specification, paragraph 0056, and Fig. 16*),

d) forming a layer of silicon-rich insulator (60) over the storage layer (50) (Step 50) (*Appellants' specification, paragraph 0056, and Fig. 16*),

e) forming a tunnel-junction layer (70) over the layer of silicon-rich insulator (60) (Step 60) (*Appellants' specification, paragraph 0056, and Fig. 16*),

f) forming and patterning a second conductive layer (40 or 30) over the tunnel-junction layer (70) (Steps 70 and 80) (*Appellants' specification, paragraph 0056, and Fig. 16*),

g) forming and patterning an interlayer dielectric (120, 340) over the storage layer (50) (Step 90) (*Appellants' specification, paragraphs 0058 and 0062, and Fig. 16, and Fig. 16*),

h) forming an opening through the interlayer dielectric (120, 340) and extending to the storage layer (50) (Step 100) (*Appellants' specification, paragraphs 0059, 0062, and 0063, and Fig. 16*), and

i) filling the opening through the interlayer dielectric (120, 340) with conductive material to form a middle electrode (130) contiguous with the storage layer (50) (Step 100) (*Appellants' specification, paragraphs 0059, 0062, and 0063, and Fig. 16*), wherein the first and second conductive layers (30 or 40) are adapted to provide exactly two terminals for control of the memory cell (20) (*Appellants' specification, paragraphs 0039, 0051, and 0052, and Figs. 3, 14, and 15*), and wherein the silicon-rich insulator (60) injects

current into the tunnel-junction layer (70) when the memory cell (20) is selected (*Appellants' specification, paragraph 0034*).

Claim 47 recites:

A multilayer memory (10) made by a method comprising:

a) providing a substrate (300) (Step 10) (*Appellants' specification, paragraph 0055, and Fig. 16*),

b) depositing and patterning a first conductive layer (30 or 40) over the substrate (300) (Steps 20 and 30) (*Appellants' specification, paragraph 0056*),

c) forming a storage layer (50) over the patterned first conductive layer (30 or 40) (Step 40) (*Appellants' specification, paragraph 0056, and Fig. 16*),

d) forming and patterning a first interlayer dielectric (120, 340) over the storage layer (50) (Step 90) (*Appellants' specification, paragraphs 0058 and 0062, and Fig. 16*),

e) forming an opening through the first interlayer dielectric (120, 340) and extending to the storage layer (50) (Step 100) (*Appellants' specification, paragraphs 0059, 0062, and 0063, and Fig. 16*),

f) filling the opening through the first interlayer dielectric (120, 340) with conductive material to form a middle electrode (130) (Step 100) (*Appellants' specification, paragraphs 0059, 0062, and 0063, and Fig. 16*),

g) forming a layer of silicon-rich insulator (60) over at least the first interlayer dielectric (120, 340), at least a portion of the silicon-rich insulator (60) being disposed contiguous with the middle electrode (130) (Step 100) (*Appellants' specification, paragraphs 0059, 0062, and 0063, and Fig. 16*),

h) forming a tunnel-junction layer (70) over the layer of silicon-rich insulator (60) (Step 60) (*Appellants' specification, paragraphs 0056, and Fig. 16*),

i) forming and patterning a second conductive layer (40 or 30) over the tunnel-junction layer (70) and disposed to overlay vertically at least a portion of the middle electrode (130) (*Appellants' specification, paragraphs 0056 and 0062*), whereby a portion of the second conductive layer (40 or 30) is aligned with some portion of the middle electrode (130) (*Appellants' specification, paragraphs 0056, 0062 and 0065*), and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory cell (20) (*Appellants' specification, paragraphs 0039, 0051, and 0052, and Figs. 3, 14, and 15*), and wherein the silicon-rich insulator (60) injects current into the tunnel-junction layer (70) when the memory cell (20) is selected (*Appellants' specification, paragraph 0034*),

j) forming and patterning a second interlayer dielectric (120, 340) over the patterned second conductive layer (40 or 30), whereby a substrate (300) is formed for subsequent layers (Step 90) (*Appellants' specification, paragraphs 0058, 0062, and 0064*),

k) forming vias (350) as required through the second interlayer dielectric (120, 340) (*Appellants' specification, paragraphs 0048, 0064, and 0065*), and

l) repeating steps b) through k) until a desired number of memory array layers have been formed (*Appellants' specification, paragraph 0064*).

Claim 55 recites:

A multilayer memory (10) made by a method comprising:

a) providing a substrate (300) (Step 10) (*Appellants' specification, paragraph 0055, and Fig. 16*),

b) depositing and patterning a first conductive layer (30 or 40) over the substrate (300) (Steps 20 and 30) (*Appellants' specification, paragraph 0056, and Fig. 16*),

c) forming a tunnel-junction layer (70) over the first conductive layer (30 or 40) (Step 60) (*Appellants' specification, paragraphs 0041, 0056, and Figs. 5-8*),

d) forming a layer of silicon-rich insulator (60) over the tunnel-junction layer (70) (Step 50) (*Appellants' specification, paragraphs 0041 and 0056, and Figs. 5-8*),

e) forming and patterning a first interlayer dielectric (120, 340) over the layer of silicon-rich insulator (60) (Step 90) (*Appellants' specification, paragraphs 0041, 0058 and 0062, and Figs. 5-8*),

f) forming an opening through the first interlayer dielectric (120, 340) and extending to the layer of silicon-rich insulator (60) (Step 100) (*Appellants' specification, paragraphs 0059, 0062, and 0063, and Fig. 16*),

g) filling the opening through the first interlayer dielectric (120, 340) with conductive material to form a middle electrode (130), at least a portion of the middle electrode (130) being disposed contiguous with the silicon-rich insulator (60) (Step 100) (*Appellants' specification, paragraphs 0059, 0062, and 0063, and Fig. 16*),

h) forming a storage-element layer over the patterned first interlayer dielectric (120, 340) (Step 40) (*Appellants' specification, paragraph 0056, and Fig. 16*),

i) forming and patterning a second conductive layer (40 or 30) over the storage-element layer (Steps 70 and 80) (*Appellants' specification, paragraph 0056, and Fig. 16*), the patterned second conductive layer (40 or 30) being disposed to overlay vertically at least a portion of the middle electrode (130) (*Appellants' specification, paragraphs 0056, 0062, and 0065*), whereby a portion of the second conductive layer (40 or 30) is aligned with some portion of the middle electrode (130) (*Appellants' specification, paragraphs 0056,*

0062, and 0065), and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory cell (20) (*Appellants' specification, paragraphs 0039, 0051, and 0052, and Figs. 3, 14, and 15*), and wherein the silicon-rich insulator (60) injects current into the tunnel-junction layer (70) when the memory cell (20) is selected (*Appellants' specification, paragraph 0034*),

j) forming and patterning a second interlayer dielectric (120, 340) over the patterned second conductive layer (40 or 30), whereby a substrate (300) is formed for subsequent layers (Step 90) (*Appellants' specification, paragraphs 0058, 0062, and 0064*),

k) forming vias (350) as required through the second interlayer dielectric (120, 340) (*Appellants' specification, paragraphs 0048, 0064, and 0065*), and

l) repeating steps b) through k) until a desired number of memory array layers have been formed (*Appellants' specification, paragraph 0064*).

VI. Grounds of Rejection to be Reviewed on Appeal

The final Office Action raised the following grounds of rejection.

(1) Claims 4-5 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

(2) Claims 1, 3-6, 8-11, 16, 26-33, 38-41, 47-49 and 55-59 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,881,994 to Lee et al. ("Lee") in view of U.S. Patent No. 7,012,297 to Bhattacharyya ("Bhattacharyya"), U.S. Patent No. 4,717,943 to Wolf et al. ("Wolf"), and U.S. Patent No. 4,870,470 to Bass Jr. et al. ("Bass").

(3) Claims 1, 3-6, 8-11, 16, 26-33, 38-41, 47-49 and 55-59 were alternatively rejected under 35 U.S.C. § 103(a) as being unpatentable over Bass in view of Lee and U.S. Patent 6,834,008 to Rinerson et al. ("Rinerson").

According, Appellant hereby requests review of each of these grounds of rejection in the present appeal.

VII. Argument

(1) Claims 4-5 complies with 35 U.S.C. § 112, second paragraph:

The final Office Action rejects claims 4-5 as being indefinite under 35 U.S.C. § 112, second paragraph. Appellant respectfully disagrees.

Claim 4:

Claim 4 recites:

> The memory array of claim 1, wherein the silicon-rich insulator of each memory cell is electrically isolated from the silicon-rich insulators of all other memory cells.

The Action offers no reasons or grounds for rejecting claim 4 as being indefinite under 35 U.S.C. § 112, second paragraph. In the absence of any indication why claim 4 is thought to be indefinite under 35 U.S.C. § 112, second paragraph, the rejection of claim 4 is improper and should not be sustained.

Claim 5:

Claim 5 recites:

> The memory array of claim 1, wherein the control element of each memory cell further comprises a tunnel junction layer thickness of about 3 – 5 nanometers.

With regard to claim 5, the Action argues that the claimed "tunnel junction layer" is unclear "as to the structural relationship between the tunnel junction layer and the memory array." (Action, p. 2).

Claim 5 depends from claim 1. Claim 1 expressly recites a memory cell disposed at each cross-point between column and row conductors. According to claim 1, each memory

cell comprises a storage element and a control element, "each control element including a tunnel junction." Claim 5 then recites that the layer of the tunnel junction has a thickness of about 3-5 nanometers. Consequently, the relationship between the tunnel junction and the memory array appears to be perfectly clear.

The Action further asserts that the claimed "tunnel junction layer thickness of about 3-5 nanometers" recited in claim 5 is "unclear as to which claimed element has the thickness of about 3-5 nanometers." (Action, p. 3). Again, claim 5 depends from claim 1, which expressly recites "each control element including a tunnel junction." (Claim 1). Because no other "tunnel junction" is recited in either of claims 1 and 5, the "tunnel junction layer thickness" recited in claim 5 can only refer to the thickness of the "tunnel junction" that is included in the "control element" recited in claim 1.

Therefore, the final Office Action has failed to indicate any indefiniteness in claim 5 under § 112, second paragraph. For at least these reasons, the rejection of claim 5 should not be sustained.

(2) Claims 1, 3-6, 8-11, 16, 26-33, 38-41, 47-49 and 55-59 are patentable over Lee, Bhattacharyya, Wolf and Bass:

Claim 1:

Claim 1 recites:

> A memory array comprising:
>
> a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and
>
> b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals and having a storage element and a control

> element coupled in series between a row conductor and a column conductor, each control element including a tunnel junction and *a silicon-rich insulator, wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected.*

(Emphasis added).

Appellant notes that in the two terminal memory cell taught in Appellant's specification, a memory cell "is selected" by applying a voltage difference between the two terminals of the memory cell. (*See e.g.,* Appellant's specification, pp. 13-14 and Figs. 14-15). During a read operation, a read voltage is applied to the terminals and an amount of current flowing between the terminals is measured with a sense amplifier. (*Id.*). During a write operation, the cell is selected by applying a write voltage differential to the terminals that is different from the read voltage to change a storage state of the storage element in the memory cell. (*See Id.* at pp. 6, 13-14 and Figs. 14-15).

In light of the above, Appellant's specification defines memory cell selection as necessarily encompassing memory cell selection during both read and write operations. Because the meaning of words used in the claims is determined by the meaning given to those words in the specification, a prior art memory cell must be evaluated during both read and write operations to determine the behavior of the memory cell when it "is selected." (Claim 1; s*ee Markman v. Westview Instruments*, 116 S. Ct. 1384 (1996); *McGill, Inc. v. John Zink Co.*, 736 F.2d 666, 674 (Fed. Cir. 1984); *ZMI Corp. v. Cardiac Resuscitator Corp.* 884 F.2d 1576, 1580, 6 U.S.P.Q.2d 1557, 1560-61 (Fed. Cir. 1988) ("words must be used in the same way in both the claims and the specification.")). Furthermore, because Appellant's specification defines a "control element" as "for controlling **write and read** operations" in a memory cell, any assertion that the prior art teaches a control element as recited in claim 1 must be evaluated in light of whether the cited prior art elements are configured to control **both** write and read operations. (Appellant's specification, p.2)

Turning now to the cited prior art, Lee, Bhattacharyya, Wolf, and Bass utterly fail to teach or suggest a memory cell having "a control element" that includes "a tunnel junction and a silicon-rich insulator, wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected." (Claim 1). The final Office Action concedes the shortcomings of Lee in this regard. Specifically, the final Office Action states that Lee does "not teach a control element including a tunnel junction and a silicon-rich oxide insulator, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected." (final Office Action, p. 4).

Consequently, the Action cites to Bhattacharyya. According to the final Office Action, Bhattacharyya teaches "a control element including a tunnel junction and a silicon-rich oxide insulator 1154, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected." (final Office Action, p. 4). Appellant respectfully disagrees.

Bhattacharyya teaches a field-effect transistor based memory cell that has three terminals—a drain, a source and a gate stack. (*See, e.g.*, Bhattacharyya at Figs. 6-14 and col. 7, lines 16-38). The gate stack includes at least "a control gate," a first "injector layer," a "charge blocking layer," a "tunnel layer," and a second "injector layer." (*Id.* at Fig. 11). The injector layers may include silicon-rich nitride (SRN) material. (*See, e.g., Id.* at col. 12, lines 11-18). A digital "1" value can be written to the memory cell of Bhattacharyya by applying a "programming voltage" to the control gate of the gate stack, thereby injecting a sufficient amount of charge into the tunnel layer of the gate stack such that a voltage difference between the gate of the field-effect transistor and the source of the field-effect transistor is maintained at a level greater than a device-characteristic threshold voltage, effectively creating a short circuit between the drain and the source of the transistor. (*See, e.g., Id.* at col. 8, lines 9-22;

Fig. 9). Similarly, a "0" is stored in the memory cell when gate stack does not store a sufficient amount of charge to create a voltage difference between the gate and the source of the transistor that is greater than the threshold voltage, thereby effectively creating an open circuit between the drain and the source of the transistor. (*Id.*).

Bhattacharyya does not explicitly describe how data is read from the memory cell it teaches. However, the processing of reading data from the three-terminal FET-based memory cells to which Bhattacharyya is directed are well-known in the art and readily apparent from the inherent physical characteristics of the cells. To read a digital value stored by the memory cell of Bhattacharyya, the memory cell must first be selected by applying a voltage difference between the drain and the source of the FET transistor. Then current flow between the drain and the source is measured, for example with one or more sense amplifiers. If the measured current flow is greater than a predetermined amount, a digital "1" is read from the memory cell. Otherwise, a digital "0" is read. No voltage can be applied to the gate stack of a FET-based memory cell during a read cycle due to the likely corruption of the data being read from the memory cell.

Appellant wishes to point out that the gate stack taught by Bhattacharyya is only used to control write operations of its associated memory cell. Read operations in the memory cell are performed independently without applying any kind of change in voltage to the gate stack or measuring a voltage or current at the gate stack. Therefore, because the gate stack of Bhattacharyya does not "[control] write and read operations" of its associated memory cell, the gate stack **cannot** read on the control element recited in claim 1. (Appellant's specification, p.2) Bhattacharyya utterly fails to teach or suggest such a control element anywhere.

Appellant further notes that even if the gate stack taught by Bhattacharyya could be considered a "control element" as defined in Appellant's specification, due to the inherent requirement that voltage be applied to the gate stack for one of the injector layers in the gate stack to inject current into the tunnel layer of the gate stack, charge cannot be injected into the tunnel layer of the gate stack when the memory cell is selected for a read operation. Therefore, Bhattacharyya does not teach or suggest the injection of charge into the tunnel layer of the gate stack when the memory cell is selected for a read operation under any circumstances. Because of Bhattacharyya's failure to teach or suggest this subject matter, Bhattacharyya **cannot** teach or suggest a memory cell having a "control element including a tunnel junction and a silicon-rich insulator, *wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected*." (Claim 1, emphasis added).

Turning now to Wolf, the final Office Action alleges that Wolf teaches "in Figure 2 and related text a control element including a tunnel junction 16 and a silicon-rich oxide insulator 20, wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected." (Action, p. 4). Appellant respectfully disagrees. Like Bhattacharyya, Wolf teaches a three-terminal FET-based memory cell having a gate stack. The gate stack includes a layer 16 of silicon dioxide that may function as a tunnel junction and a layer 20 of silicon-rich oxide disposed between the layer 16 of silicon dioxide and an upper electrode 12. (Wolf, col. 2, lines 36-45 and 55-65). However, like Bhattacharyya, the three-terminal memory cell taught by Wolf follows the well-known conventions of three-terminal FET-based memory cells in the art, in that the memory cell is selected for a read operation by applying a voltage difference between a drain and a source in the FET, during which time voltage may not be applied to the gate stack. (*See* Wolf, col. 2, lines 15-20).

Therefore, like its counterpart in Bhattacharyya, the gate stack taught by Wolf is only used to control write operations of its associated memory cell. Read operations in the memory cell are performed independently without applying any kind of change in voltage to the gate stack or measuring a voltage or current at the gate stack. Therefore, because the gate stack of Wolf does not "[control] write and read operations" of its associated memory cell, the gate stack **cannot** read on the control element recited in claim 1. (Appellant's specification, p.2) Wolf utterly fails to teach or suggest such a control element anywhere.

Furthermore, because voltage is not applied to the gate stack of the memory cell taught by Wolf when the memory cell is selected for a read operation, the layer 20 of silicon-rich oxide in the gate stack *cannot* inject current into the tunnel junction 16 of the gate stack when the memory cell is selected for a read operation. Moreover, Wolf does not teach or suggest anywhere that the layer 20 of silicon-rich oxide in the gate stack injects current into the tunnel junction 16 when the memory cell is selected for a read operation. Accordingly, Wolf **cannot** teach or suggest a memory cell having a "control element including a tunnel junction and a silicon-rich insulator, *wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected*." (Claim 1, emphasis added).

Turning now to Bass, the final Office Action alleges that Bass "teach[es] in Figure 6 and related text a control element including a tunnel junction and a silicon-rich insulator 35, wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected." (Action, p. 4). Appellant respectfully disagrees.

Appellant notes that Bass, like Bhattacharyya and Wolf, is directed to a three-terminal FET-based memory cell having a gate stack configured to store charge according to the digital value written to the memory cell. The gate stack of Bass includes a silicon-rich silicon nitride film 30 deposited on top of a silicon oxide layer 20 and having a barrier layer 25 formed on

the silicon-rich silicon nitride film, and a charge injection structure 35 deposited on the barrier layer 25. (Bass, col. 7, lines 40-57; col. 8, lines 3-4; Fig. 6).

The gate stack taught by Bass, just like its counterparts in Bhattacharyya and Wolf, is only used to control write operations of its associated memory cell. Read operations in the memory cell are performed independently without applying any kind of change in voltage to the gate stack or measuring a voltage or current at the gate stack. Therefore, because the gate stack of Bass does not "[control] write and read operations" of its associated memory cell, the gate stack **cannot** read on the control element recited in claim 1. (Appellant's specification, p.2) Bass utterly fails to teach or suggest such a control element anywhere.

Moreover, Bass does not teach anywhere that the silicon-rich silicon nitride film 30 injects current into either the silicon oxide layer 20 or the barrier layer 25 when the memory cell is selected for a read process. Further, such current injection could not occur while maintaining reliable functionality of the memory cell of Bass for the reasons given above with respect to the analogous three-terminal FET-based memory cells taught by Bhattacharyya and Wolf. Accordingly, Bass **cannot** teach or suggest a memory cell having a "control element including a tunnel junction and a silicon-rich insulator, *wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected*." (Claim 1, emphasis added).

The Supreme Court recently addressed the issue of obviousness in *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727 (2007). The Court stated that the *Graham v. John Deere Co. of Kansas City*, 383, U.S. 1 (1966), factors still control an obviousness inquiry. Under the analysis required by *Graham v. John Deere*, 383 U.S. 1 (1966) to support a rejection under § 103, the scope and content of the prior art must first be determined, followed by an

assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art.

In the present case, the scope and content of the prior art, as evidenced by Lee, Bhattacharyya, Wolf, and Bass, did not include the claimed subject matter, particularly the claimed memory cell comprising a control element with a tunnel junction and a silicon-rich insulator that injects current into the tunnel junction when the memory cell is selected. This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 1 and its dependent claims based on Lee, Bhattacharyya, Wolf, and Bass should not be sustained in view of 35 U.S.C. § 103 and *Graham*.

Claim 4:

Claim 4 recites:

> The memory array of claim 1, wherein the silicon-rich insulator of each memory cell is *electrically isolated from the silicon-rich insulators of all other memory cells*.

(Emphasis added).

With regard to claim 4, the final Acton fails to cite to any support for the rejection of claim 4 in any of the prior art references, Lee, Bhattacharyya, Wolf, or Bass. Consequently, no *prima facie* case of obviousness has been made against claim 4, and the rejection of claim 4 should not be sustained.

Claim 6:

Claim 6 recites "wherein the storage element of each memory cell comprises an anti-fuse." The final Office Action fails to specifically address claim 6 and does not indicate how or where this subject matter is taught or suggested by the prior art of record. Consequently, no *prima facie* case of obviousness has been made against claim 6, and the rejection of claim 6 should not be sustained.

Claims 9 and 10:

Claims 9 and 10 recite, respectively, that "the storage element of each memory cell comprises a state-change layer" and "wherein the state-change layer of the storage element comprises a chalcogenide." The final Office Action fails to specifically address claims 9 and 10 and does not indicate how or where this subject matter is taught or suggested by the prior art of record. Consequently, no *prima facie* case of obviousness has been made against claims 9 and 10, and the rejection of claims 9 and 10 should not be sustained.

Claim16:

Claim 16 recites:

> A memory array comprising:
>
> a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and
>
> b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals, each memory cell comprising means for storing data and means for controlling the means for storing data, the means for storing data and means for controlling being coupled in series between a row conductor and a column conductor, each means for controlling including a tunnel junction and *a silicon-rich insulator,*

wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected.

(Emphasis added).

As demonstrated above in connection with claim 1, Lee, Bhattacharyya, Wolf, and Bass utterly fail to teach or suggest this subject matter of a "silicon-rich insulator [that] injects current into the tunnel junction when the memory cell is selected."

Again, under the analysis required by *Graham v. John Deere*, 383 U.S. 1 (1966) to support a rejection under § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. In the present case, the scope and content of the prior art, as evidenced by Lee, Bhattacharyya, Wolf, and Bass, did not include the claimed subject matter, particularly the claimed memory cell comprising means for controlling that comprises a silicon-rich insulator that injects current into a tunnel junction when the memory cell is selected. This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 16 and its dependent claims based on Lee, Bhattacharyya, Wolf, and Bass should not be sustained in view of 35 U.S.C. § 103 and *Graham*.

Claim 26:

Claim 26 recites:

> A memory cell made by a method comprising:
>
> a) providing a substrate,
>
> b) depositing and patterning a first conductive layer over the substrate,
>
> c) forming a storage layer over the patterned first conductive layer,
>
> d) forming a layer of silicon-rich insulator over the storage layer,
>
> e) forming a tunnel-junction layer over the layer of silicon-rich insulator, and
>
> f) forming and patterning a second conductive layer over the tunnel-junction layer, whereby a memory-cell stack is formed, the stack having a storage layer, a silicon-rich insulator, and a tunnel-junction layer in series relationship between the first and second conductive layers, whereby the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell, *wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected.*

(Emphasis added).

As demonstrated above in connection with claim 1, Lee, Bhattacharyya, Wolf, and Bass utterly fail to teach or suggest this subject matter of a memory cell that comprises a silicon-rich insulator, and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected."

Again, under the analysis required by *Graham v. John Deere*, 383 U.S. 1 (1966) to support a rejection under § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. In the present case, the scope and content of the prior art, as evidenced by Lee, Bhattacharyya, Wolf, and Bass, did not include the claimed subject matter, particularly the claimed memory cell comprising a silicon-rich insulator that injects current into a tunnel junction when the memory cell is selected. This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 26 and its dependent claims based on Lee, Bhattacharyya, Wolf, and Bass should not be sustained in view of 35 U.S.C. § 103 and *Graham*.

Claim 38:

Claim 38 recites:

> A memory cell made by a method comprising:
>
> a) providing a substrate,
>
> b) depositing and patterning a first conductive layer over the substrate,
>
> c) forming a storage layer over the patterned first conductive layer,
>
> d) forming a layer of silicon-rich insulator over the storage layer,
>
> e) forming a tunnel-junction layer over the layer of silicon-rich insulator,
>
> f) forming and patterning a second conductive layer over the tunnel-junction layer,
>
> g) forming and patterning an interlayer dielectric over the storage layer,
>
> h) forming an opening through the interlayer dielectric and extending to the storage layer, and
>
> i) filling the opening through the interlayer dielectric with conductive material to form a middle electrode contiguous with the storage layer, wherein the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell, *and wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected*.

(Emphasis added).

As demonstrated above in connection with claim 1, Lee, Bhattacharyya, Wolf, and Bass utterly fail to teach or suggest this subject matter of a memory cell that comprises a

silicon-rich insulator, and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected."

Again, under the analysis required by *Graham v. John Deere*, 383 U.S. 1 (1966) to support a rejection under § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. In the present case, the scope and content of the prior art, as evidenced by Lee, Bhattacharyya, Wolf, and Bass, did not include the claimed subject matter, particularly the claimed memory cell comprising a silicon-rich insulator that injects current into a tunnel junction when the memory cell is selected. This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 38 and its dependent claims based on Lee, Bhattacharyya, Wolf, and Bass should not be sustained in view of 35 U.S.C. § 103 and *Graham*.

Claim 47:

Claim 47 recites:

> A multilayer memory made by a method comprising:
> a) providing a substrate,
> b) depositing and patterning a first conductive layer over the substrate,
> c) forming a storage layer over the patterned first conductive layer,
> d) forming and patterning a first interlayer dielectric over the storage layer,
> e) forming an opening through the first interlayer dielectric and extending to the storage layer,

f) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode,

g) forming a layer of silicon-rich insulator over at least the first interlayer dielectric, at least a portion of the silicon-rich insulator being disposed contiguous with the middle electrode,

h) forming a tunnel-junction layer over the layer of silicon-rich insulator,

i) forming and patterning a second conductive layer over the tunnel junction layer and disposed to overlay vertically at least a portion of the middle electrode, whereby a portion of the second conductive layer is aligned with some portion of the middle electrode, and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory cell, and *wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected*,

j) forming and patterning a second interlayer dielectric over the patterned second conductive layer, whereby a substrate is formed for subsequent layers,

k) forming vias as required through the second interlayer dielectric, and

l) repeating steps b) through k) until a desired number of memory array layers have been formed.

(Emphasis added).

As demonstrated above in connection with claim 1, Lee, Bhattacharyya, Wolf, and Bass utterly fail to teach or suggest this subject matter of a memory cell that comprises a silicon-rich insulator, and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected."

Again, under the analysis required by *Graham v. John Deere*, 383 U.S. 1 (1966) to support a rejection under § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. In the present case, the scope and content of the prior art, as evidenced by Miyasaka and Udayakumar, did not include the claimed subject matter, particularly the claimed memory cell comprising a silicon-rich insulator that injects

current into a tunnel junction when the memory cell is selected. This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 47 and its dependent claims based on Lee, Bhattacharyya, Wolf, and Bass should not be sustained in view of 35 U.S.C. § 103 and *Graham*.

Claim 55:

Claim 55 recites:

> A multilayer memory made by a method comprising:
>
> a) providing a substrate,
>
> b) depositing and patterning a first conductive layer over the substrate,
>
> c) forming a tunnel-junction layer over the first conductive layer,
>
> d) forming a layer of silicon-rich insulator over the tunnel-junction layer,
>
> e) forming and patterning a first interlayer dielectric over the layer of silicon-rich insulator,
>
> f) forming an opening through the first interlayer dielectric and extending to the layer of silicon-rich insulator,
>
> g) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode, at least a portion of the middle electrode being disposed contiguous with the silicon-rich insulator,
>
> h) forming a storage-element layer over the patterned first interlayer dielectric,
>
> i) forming and patterning a second conductive layer over the storage element layer, the patterned second conductive layer being disposed to overlay vertically at least a portion of the middle electrode, whereby a portion of the second conductive layer is aligned with some portion of the middle electrode, and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory cell, and *wherein the silicon-*

rich insulator injects current into the tunnel-junction layer when the memory cell is selected,

j) forming and patterning a second interlayer dielectric over the patterned second conductive layer, whereby a substrate is formed for subsequent layers,

k) forming vias as required through the second interlayer dielectric, and

l) repeating steps b) through k) until a desired number of memory array layers have been formed.

(Emphasis added).

As demonstrated above in connection with claim 1, Lee, Bhattacharyya, Wolf, and Bass utterly fail to teach or suggest this subject matter of a memory cell that comprises a silicon-rich insulator, and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected."

Again, under the analysis required by *Graham v. John Deere*, 383 U.S. 1 (1966) to support a rejection under § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. In the present case, the scope and content of the prior art, as evidenced by Lee, Bhattacharyya, Wolf, and Bass, did not include the claimed subject matter, particularly the claimed memory cell comprising a silicon-rich insulator that injects current into a tunnel junction when the memory cell is selected. This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 1 and its dependent claims based on Lee, Bhattacharyya, Wolf, and Bass should not be sustained in view of 35 U.S.C. § 103 and *Graham*.

(3) Claims 1, 3-6, 8-11, 16, 26-33, 38-41, 47-49 and 55-59 are patentable over Bass, Lee, and Rinerson:

Claim 1:

Claim 1 recites:

> A memory array comprising:
>
> a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and
>
> b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals and having a storage element and a control element coupled in series between a row conductor and a column conductor, each control element including a tunnel junction and *a silicon-rich insulator, wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected.*

(Emphasis added).

Appellant again notes that in the two terminal memory cell taught in Appellant's specification, a memory cell "is selected" by applying a voltage difference between the two terminals of the memory cell. (*See e.g.,* Appellant's specification, pp. 13-14 and Figs. 14-15). During a read operation, a read voltage is applied to the terminals and an amount of current flowing between the terminals is measured with a sense amplifier. (*Id.*). During a write operation, the cell is selected by applying a write voltage differential to the terminals that is different from the read voltage to change a storage state of the storage element in the memory cell. (*See Id.* at pp. 6, 13-14 and Figs. 14-15).

In light of the above, Appellant's specification defines memory cell selection as necessarily encompassing memory cell selection during both read and write operations. Because the meaning of words used in the claims is determined by the meaning given to those

words in the specification, a prior art memory cell must be evaluated during both read and write operations to determine the behavior of the memory cell when it "is selected." (Claim 1; S*ee Markman v. Westview Instruments*, 116 S. Ct. 1384 (1996); *McGill, Inc. v. John Zink Co.*, 736 F.2d 666, 674 (Fed. Cir. 1984); *ZMI Corp. v. Cardiac Resuscitator Corp.* 884 F.2d 1576, 1580, 6 U.S.P.Q.2d 1557, 1560-61 (Fed. Cir. 1988) ("words must be used in the same way in both the claims and the specification.")). Furthermore, because Appellant's specification defines a "control element" as "for controlling **write and read** operations" in a memory cell, any assertion that the prior art teaches a control element as recited in claim 1 must be evaluated in light of whether the cited prior art elements are configured to control **both** write and read operations. (Appellant's specification, p.2)

Turning now to the cited prior art, each of Bass, Lee, and Rinerson utterly fails to teach or suggest a memory cell having "a control element" that includes "a tunnel junction and a silicon-rich insulator, wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected." (Claim 1). The final Office Action concedes the shortcomings of Lee in this regard. Specifically, the final Office Action states that Lee does "not teach a control element including a tunnel junction and a silicon-rich oxide insulator, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected." (final Office Action, p. 4).

Turning now to Bass, the final Office Action alleges that Bass "teach[es] in Figure 6 and related text a control element including a tunnel junction and a silicon-rich insulator 35, wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected." (Action, p. 4). Appellant respectfully disagrees.

Appellant notes that Bass, as has been amply discussed above with respect to the above alternative grounds of rejection, is directed to a three-terminal FET-based memory cell

having a gate stack configured to store charge according to the digital value written to the memory cell. The gate stack of Bass includes a silicon-rich silicon nitride film 30 deposited on top of a silicon oxide layer 20 and having a barrier layer 25 formed on the silicon-rich silicon nitride film, and a charge injection structure 35 deposited on the barrier layer 25. (Bass, col. 7, lines 40-57; col. 8, lines 3-4; Fig. 6).

The gate stack taught by Bass is only used to control write operations of its associated memory cell. Read operations in the memory cell are performed independently without applying any kind of change in voltage to the gate stack or measuring a voltage or current at the gate stack. Therefore, because the gate stack of Bass does not "[control] write and read operations" of its associated memory cell, the gate stack **cannot** read on the control element recited in claim 1. (Appellant's specification, p.2) Bass utterly fails to teach or suggest such a control element anywhere.

Moreover, Bass does not teach anywhere that the silicon-rich silicon nitride film 30 injects current into either the silicon oxide layer 20 or the barrier layer 25 when the memory cell is selected for a read process. Further, such current injection could not occur while maintaining reliable functionality of the memory cell of Bass for the reasons given above with respect to the analogous three-terminal FET-based memory cells taught by Bhattacharyya and Wolf. Accordingly, Bass **cannot** teach or suggest a memory cell having a "control element including a tunnel junction and a silicon-rich insulator, *wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected*." (Claim 1, emphasis added).

Rinerson teaches a "cross point memory array" that "includes a first layer of conductive array lines, a second layer of conductive array lines and a plurality of memory plugs." (Rinerson, col. 2, lines 12-15). Each of the memory plugs "has a memory element

that, in a first write mode, switches from a first resistance state to a second resistance state upon application of a first write voltage" and "[i]n a second write mode…reversibly switches from the second resistance state back to the first resistance state upon application of a second write voltage." (*Id.* at lines 26-33).

The final Office Action makes no allegation that Rinerson teaches the control element recited in claim 1. Appellant notes that an examination of Rinerson readily reveals that Rinerson utterly fails to teach or suggest the use of "silicon-rich insulator" or a "tunnel junction" anywhere, let alone a "control element including a tunnel junction and a silicon-rich insulator, *wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected*." (Claim 1, emphasis added)."

Again, under the analysis required by *Graham v. John Deere*, 383 U.S. 1 (1966) to support a rejection under § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. In the present case, the scope and content of the prior art, as evidenced by Bass, Lee, and Rinerson, did not include the claimed subject matter, particularly the claimed memory cell comprising a control element with a tunnel junction and a silicon-rich insulator that injects current into the tunnel junction when the memory cell is selected. This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 1 and

its dependent claims based on Bass, Lee, and Rinerson should not be sustained in view of 35 U.S.C. § 103 and *Graham*.

Claim 4:

Claim 4 recites:

> The memory array of claim 1, wherein the silicon-rich insulator of each memory cell *is electrically isolated from the silicon-rich insulators of all other memory cells*.

(Emphasis added).

With regard to claim 4, the final Acton fails to cite to any support for the rejection of claim 4 in any of the prior art references, Bass, Lee, or Rinerson. Consequently, no *prima facie* case of obviousness has been made against claim 4, and the rejection of claim 4 should not be sustained.

Claim 6:

Claim 6 recites "wherein the storage element of each memory cell comprises an anti-fuse." The final Office Action fails to specifically address claim 6 and does not indicate how or where this subject matter is taught or suggested by the prior art of record. Consequently, no *prima facie* case of obviousness has been made against claim 6, and the rejection of claim 6 should not be sustained.

Claims 9 and 10:

Claims 9 and 10 recite, respectively, that "the storage element of each memory cell comprises a state-change layer" and "wherein the state-change layer of the storage element comprises a chalcogenide." The final Office Action fails to specifically address claims 9 and

10 and does not indicate how or where this subject matter is taught or suggested by the prior art of record. Consequently, no *prima facie* case of obviousness has been made against claims 9 and 10, and the rejection of claims 9 and 10 should not be sustained.

Claim16:

Claim 16 recites:

> A memory array comprising:
>
> a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and
>
> b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals, each memory cell comprising means for storing data and means for controlling the means for storing data, the means for storing data and means for controlling being coupled in series between a row conductor and a column conductor, each means for controlling including a tunnel junction and *a silicon-rich insulator, wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected.*

(Emphasis added).

As demonstrated above in connection with claim 1, Bass, Lee, and Rinerson utterly fail to teach or suggest this subject matter of a "silicon-rich insulator [that] injects current into the tunnel junction when the memory cell is selected."

Again, under the analysis required by *Graham v. John Deere*, 383 U.S. 1 (1966) to support a rejection under § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. In the present case, the scope and content of the prior art, as evidenced by Bass, Lee, and Rinerson, did not include the claimed subject matter, particularly the claimed memory cell comprising means for controlling that comprises a silicon-rich insulator that injects current into a tunnel junction when the memory cell is selected. This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 16 and its dependent claims based on Bass, Lee, and Rinerson should not be sustained in view of 35 U.S.C. § 103 and *Graham*.

Claim 26:

Claim 26 recites:

> A memory cell made by a method comprising:
>
> a) providing a substrate,
>
> b) depositing and patterning a first conductive layer over the substrate,
>
> c) forming a storage layer over the patterned first conductive layer,
>
> d) forming a layer of silicon-rich insulator over the storage layer,
>
> e) forming a tunnel-junction layer over the layer of silicon-rich insulator, and
>
> f) forming and patterning a second conductive layer over the tunnel-junction layer, whereby a memory-cell stack is formed, the stack having a storage layer, a silicon-rich insulator, and a tunnel-junction layer in series relationship between the first and second conductive layers, whereby the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell, *wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected.*

(Emphasis added).

As demonstrated above in connection with claim 1, Lee, Bhattacharyya, Wolf, and Bass utterly fail to teach or suggest this subject matter of a memory cell that comprises a silicon-rich insulator, and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected."

Again, under the analysis required by *Graham v. John Deere*, 383 U.S. 1 (1966) to support a rejection under § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. In the present case, the scope and content of the prior art, as evidenced by Bass, Lee, and Rinerson, did not include the claimed subject matter, particularly the claimed memory cell comprising a silicon-rich insulator that injects current into a tunnel junction when the memory cell is selected. This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 26 and its dependent claims based on Bass, Lee, and Rinerson should not be sustained in view of 35 U.S.C. § 103 and *Graham*.

Claim 38:

Claim 38 recites:

> A memory cell made by a method comprising:
>
> a) providing a substrate,
>
> b) depositing and patterning a first conductive layer over the substrate,
>
> c) forming a storage layer over the patterned first conductive layer,
>
> d) forming a layer of silicon-rich insulator over the storage layer,
>
> e) forming a tunnel-junction layer over the layer of silicon-rich insulator,
>
> f) forming and patterning a second conductive layer over the tunnel-junction layer,
>
> g) forming and patterning an interlayer dielectric over the storage layer,

> h) forming an opening through the interlayer dielectric and extending to the storage layer, and
>
> i) filling the opening through the interlayer dielectric with conductive material to form a middle electrode contiguous with the storage layer, wherein the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell, *and wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected*.

(Emphasis added).

As demonstrated above in connection with claim 1, Bass, Lee, and Rinerson utterly fail to teach or suggest this subject matter of a memory cell that comprises a silicon-rich insulator, and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected."

Again, under the analysis required by *Graham v. John Deere*, 383 U.S. 1 (1966) to support a rejection under § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. In the present case, the scope and content of the prior art, as evidenced by Bass, Lee, and Rinerson, did not include the claimed subject matter, particularly the claimed memory cell comprising a silicon-rich insulator that injects current into a tunnel junction when the memory cell is selected. This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 38 and its dependent claims based on Bass, Lee, and Rinerson should not be sustained in view of 35 U.S.C. § 103 and *Graham*.

Claim 47:

Claim 47 recites:

> A multilayer memory made by a method comprising:
>
> a) providing a substrate,
>
> b) depositing and patterning a first conductive layer over the substrate,
>
> c) forming a storage layer over the patterned first conductive layer,
>
> d) forming and patterning a first interlayer dielectric over the storage layer,
>
> e) forming an opening through the first interlayer dielectric and extending to the storage layer,
>
> f) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode,
>
> g) forming a layer of silicon-rich insulator over at least the first interlayer dielectric, at least a portion of the silicon-rich insulator being disposed contiguous with the middle electrode,
>
> h) forming a tunnel-junction layer over the layer of silicon-rich insulator,
>
> i) forming and patterning a second conductive layer over the tunnel junction layer and disposed to overlay vertically at least a portion of the middle electrode, whereby a portion of the second conductive layer is aligned with some portion of the middle electrode, and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory cell, and *wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected*,
>
> j) forming and patterning a second interlayer dielectric over the patterned second conductive layer, whereby a substrate is formed for subsequent layers,
>
> k) forming vias as required through the second interlayer dielectric, and
>
> l) repeating steps b) through k) until a desired number of memory array layers have been formed.

(Emphasis added).

As demonstrated above in connection with claim 1, Lee Bass, Lee, and Rinerson utterly fail to teach or suggest this subject matter of a memory cell that comprises a silicon-rich insulator, and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected."

Again, under the analysis required by *Graham v. John Deere*, 383 U.S. 1 (1966) to support a rejection under § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. In the present case, the scope and content of the prior art, as evidenced by Bass, Lee, and Rinerson, did not include the claimed subject matter, particularly the claimed memory cell comprising a silicon-rich insulator that injects current into a tunnel junction when the memory cell is selected. This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 47 and its dependent claims based on Bass, Lee, and Rinerson should not be sustained in view of 35 U.S.C. § 103 and *Graham*.

Claim 55:

Claim 55:

Claim 55 recites:

> A multilayer memory made by a method comprising:
>
> a) providing a substrate,
>
> b) depositing and patterning a first conductive layer over the substrate,
>
> c) forming a tunnel-junction layer over the first conductive layer,
>
> d) forming a layer of silicon-rich insulator over the tunnel-junction layer,
>
> e) forming and patterning a first interlayer dielectric over the layer of silicon-rich insulator,

f) forming an opening through the first interlayer dielectric and extending to the layer of silicon-rich insulator,

g) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode, at least a portion of the middle electrode being disposed contiguous with the silicon-rich insulator,

h) forming a storage-element layer over the patterned first interlayer dielectric,

i) forming and patterning a second conductive layer over the storage element layer, the patterned second conductive layer being disposed to overlay vertically at least a portion of the middle electrode, whereby a portion of the second conductive layer is aligned with some portion of the middle electrode, and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory cell, and *wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected*,

j) forming and patterning a second interlayer dielectric over the patterned second conductive layer, whereby a substrate is formed for subsequent layers,

k) forming vias as required through the second interlayer dielectric, and

l) repeating steps b) through k) until a desired number of memory array layers have been formed.

(Emphasis added).

As demonstrated above in connection with claim 1, Lee, Bhattacharyya, Wolf, and Bass utterly fail to teach or suggest this subject matter of a memory cell that comprises a silicon-rich insulator, and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected."

Again, under the analysis required by *Graham v. John Deere*, 383 U.S. 1 (1966) to support a rejection under § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. In the present case, the scope and content of the prior art, as evidenced by Lee, Bhattacharyya, Wolf, and Bass, did not include the claimed subject matter, particularly the claimed memory cell comprising a silicon-rich insulator that

injects current into a tunnel junction when the memory cell is selected. This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 1 and its dependent claims based on Bass, Lee, and Rinerson should not be sustained in view of 35 U.S.C. § 103 and *Graham*.

In view of the foregoing, it is submitted that the final rejection of the pending claims is improper and should not be sustained. Therefore, a reversal of the Rejection of October 21, 2008 is respectfully requested.

Respectfully submitted,

DATE: January 20, 2009

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VIII. CLAIMS APPENDIX

1. (Previously Presented) A memory array comprising:

a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and

b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals and having a storage element and a control element coupled in series between a row conductor and a column conductor, each control element including a tunnel junction and a silicon-rich insulator, wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected.

2. (Withdrawn) The memory array of claim 1, wherein the silicon-rich insulator of each memory cell is patterned.

3. (Original) The memory array of claim 1, wherein the silicon-rich insulator of each memory cell comprises silicon-rich oxide (SRO).

4. (Original) The memory array of claim 1, wherein the silicon-rich insulator of each memory cell is electrically isolated from the silicon-rich insulators of all other memory cells.

5. (Previously Presented) The memory array of claim 1, wherein the control element of each memory cell further comprises a tunnel junction layer thickness of about 3 – 5 nanometers.

6. (Original) The memory array of claim 1, wherein the storage element of each memory cell comprises an anti-fuse.

7. (Cancelled)

8. (Original) The memory array of claim 1, wherein the storage element of each memory cell comprises a tunnel junction.

9. (Original) The memory array of claim 1, wherein the storage element of each memory cell comprises a state-change layer.

10. (Original) The memory array of claim 9, wherein the state-change layer of the storage element comprises a chalcogenide.

11. (Original) The memory array of claim 1, wherein the row conductors are arranged in mutually orthogonal relationship with the column conductors.

12. (Withdrawn) A memory array comprising:

a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors arranged to cross at cross-points, and

b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals and having a storage element and a control element coupled in series between a row conductor and a column conductor,

each storage element comprising a tunnel-junction anti-fuse, and

each control element comprising a patterned silicon-rich insulator and a tunnel junction.

13. (Withdrawn) A memory cell comprising:

a storage element comprising a tunnel-junction anti-fuse, and

a control element coupled in series with the storage element, the control element comprising a patterned silicon-rich insulator and a tunnel junction.

14. (Withdrawn) The memory cell of claim 13, wherein the patterned silicon-rich insulator of the control element injects current into the tunnel junction of the control element when the memory cell is selected and isolates the storage element when the memory cell is unselected.

15. (Withdrawn) A memory array comprising:

a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors arranged to cross at cross-points, and

the memory cell of claim 13 disposed at each cross-point.

16. (Previously Presented) A memory array comprising:

a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and

b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals, each memory cell comprising means for storing data and means for controlling the means for storing data, the means for storing data and means for controlling being coupled in

series between a row conductor and a column conductor, each means for controlling including a tunnel junction and a silicon-rich insulator, wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected.

17. (Withdrawn) A method for controlling a memory cell of the type having an anti-fuse storage element, the method comprising the steps of:

a) providing a patterned silicon-rich insulator combined with a tunnel junction to form a control element, whereby the memory cell is isolated when unselected,

b) coupling the control element in series with the anti-fuse storage element, and

c) providing conductive elements for supplying current to selectively inject current from the silicon-rich insulator into the tunnel junction of the control element when selecting the memory cell, wherein the memory cell has exactly two terminals.

18. (Withdrawn) A memory cell controlled in accordance with the method of claim 17.

19. (Withdrawn) A memory array comprising:

a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors arranged to cross at cross-points, and

the memory cell of claim 18 disposed at each cross-point.

20. (Withdrawn) A method for fabricating a memory cell, the method comprising the steps of:

a) providing a substrate,

b) depositing and patterning a first conductive layer over the substrate,

c) forming a storage layer,

d) forming a layer of silicon-rich insulator,

e) forming a tunnel-junction layer over the layer of silicon-rich insulator, and

f) forming and patterning a second conductive layer over the tunnel-junction layer, wherein the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell.

21. (Withdrawn) The method of claim 20, further comprising the step of patterning the layer of silicon-rich insulator.

22. (Withdrawn) The method of claim 20, further comprising the step of depositing an interlayer dielectric (ILD).

23. (Withdrawn) The method of claim 22, further comprising the step of planarizing the interlayer dielectric (ILD).

24. (Withdrawn) The method of claim 20, further comprising the step of forming a conductive electrode disposed contiguous with the layer of silicon-rich insulator.

25. (Withdrawn) The method of claim 24, further comprising the step of patterning the conductive electrode.

26. (Previously Presented) A memory cell made by a method comprising:

a) providing a substrate,

b) depositing and patterning a first conductive layer over the substrate,

c) forming a storage layer over the patterned first conductive layer,

d) forming a layer of silicon-rich insulator over the storage layer,

e) forming a tunnel-junction layer over the layer of silicon-rich insulator, and

f) forming and patterning a second conductive layer over the tunnel-junction layer, whereby a memory-cell stack is formed, the stack having a storage layer, a silicon-rich insulator, and a tunnel-junction layer in series relationship between the first and second conductive layers, whereby the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell, wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected.

27. (Original) A memory array comprising a multiplicity of the memory cells of claim 26.

28. (Original) A substrate carrying electronics comprising the memory array of claim 27.

29. (Original) An integrated circuit comprising the memory array of claim 27.

30. (Original) A multilayer memory comprising:

a) a multiplicity of the memory arrays of claim 27, arranged in memory layers,

b) a multiplicity of interlayer dielectrics disposed to separate adjacent memory layers, and

c) conductive vias selectively extending through the interlayer dielectrics to selectively interconnect memory cells of the memory arrays.

31. (Original) A substrate carrying electronics comprising the multilayer memory of claim 30.

32. (Original) An integrated circuit comprising the multilayer memory of claim 30.

33. (Previously Presented) The multilayer memory of claim 30, wherein the memory cells of the multilayer memory are organized in sets, the memory cells of each set being disposed to overlay vertically at least a portion of an adjacent set, whereby some portion of the memory cells of each set are aligned vertically with each other.

34-35. (Cancelled)

36. (Withdrawn) A method for fabricating a multilayer memory, the method comprising the steps of:

i) performing the steps of claim 20 to form a first memory layer,

ii) depositing an interlayer dielectric, whereby a substrate for a subsequent memory layer is formed,

iii) performing steps b) through f) of claim 20, and

iv) repeating steps ii) and iii) until a desired number of memory layers is formed.

37. (Withdrawn) The method of claim 20, further comprising the steps of:

g) forming and patterning an interlayer dielectric over the storage layer,

h) forming an opening through the interlayer dielectric and extending to the storage layer, and

i) filling the opening through the interlayer dielectric with conductive material to form a middle electrode contiguous with the storage layer.

38. (Previously Presented) A memory cell made by a method comprising:

a) providing a substrate,

b) depositing and patterning a first conductive layer over the substrate,

c) forming a storage layer over the patterned first conductive layer,

d) forming a layer of silicon-rich insulator over the storage layer,

e) forming a tunnel-junction layer over the layer of silicon-rich insulator,

f) forming and patterning a second conductive layer over the tunnel-junction layer,

g) forming and patterning an interlayer dielectric over the storage layer,

h) forming an opening through the interlayer dielectric and extending to the storage layer, and

i) filling the opening through the interlayer dielectric with conductive material to form a middle electrode contiguous with the storage layer, wherein the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell, and wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected.

39. (Original) A memory array comprising a multiplicity of the memory cells of claim 38.

40. (Original) A substrate carrying electronics comprising the memory array of claim 39.

41. (Original) An integrated circuit comprising the memory array of claim 39.

42. (Withdrawn) A method for fabricating a multilayer memory, the method comprising the steps of:

a) providing a substrate,

b) depositing and patterning a first conductive layer over the substrate,

c) forming a storage layer,

d) forming and patterning a first interlayer dielectric over the storage layer,

e) forming an opening through the first interlayer dielectric and extending to the storage layer,

f) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode,

g) forming a layer of silicon-rich insulator, at least a portion of the silicon-rich insulator being disposed contiguous with the middle electrode,

h) forming a tunnel-junction layer over the layer of silicon-rich insulator,

i) forming and patterning a second conductive layer over the tunnel-junction layer and disposed to overlay vertically at least a portion of the middle electrode, whereby the second conductive layer is at least partially aligned with the middle electrode, and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell,

j) forming and patterning a second interlayer dielectric, whereby a substrate is formed for subsequent layers,

k) forming vias as required through the second interlayer dielectric, and

l) repeating steps b) through k) until a desired number of memory array layers have been formed.

43. (Withdrawn) The method of claim 42, further comprising the step of patterning the layer of silicon-rich insulator.

44. (Withdrawn) The method of claim 42, further comprising the step of planarizing the first interlayer dielectric.

45. (Withdrawn) The method of claim 42, further comprising the step of planarizing the second interlayer dielectric.

46. (Withdrawn) The method of claim 42, wherein the steps are performed in the order recited.

47. (Previously Presented) A multilayer memory made by a method comprising:

a) providing a substrate,

b) depositing and patterning a first conductive layer over the substrate,

c) forming a storage layer over the patterned first conductive layer,

d) forming and patterning a first interlayer dielectric over the storage layer,

e) forming an opening through the first interlayer dielectric and extending to the storage layer,

f) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode,

g) forming a layer of silicon-rich insulator over at least the first interlayer dielectric, at least a portion of the silicon-rich insulator being disposed contiguous with the middle electrode,

h) forming a tunnel-junction layer over the layer of silicon-rich insulator,

i) forming and patterning a second conductive layer over the tunnel-junction layer and disposed to overlay vertically at least a portion of the middle electrode, whereby a portion of the second conductive layer is aligned with some portion of the middle electrode, and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory cell, and wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected,

j) forming and patterning a second interlayer dielectric over the patterned second conductive layer, whereby a substrate is formed for subsequent layers,

k) forming vias as required through the second interlayer dielectric, and

l) repeating steps b) through k) until a desired number of memory array layers have been formed.

48. (Original) A substrate carrying electronics comprising the multilayer memory of claim 47.

49. (Original) An integrated circuit comprising the multilayer memory of claim 47.

50. (Withdrawn) A method for fabricating a multilayer memory, the method comprising the steps of:

a) providing a substrate,

b) depositing and patterning a first conductive layer over the substrate,

c) forming a tunnel-junction layer over the first conductive layer,

d) forming a layer of silicon-rich insulator,

e) forming and patterning a first interlayer dielectric over the layer of silicon-rich insulator,

f) forming an opening through the first interlayer dielectric and extending to the layer of silicon-rich insulator,

g) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode, at least a portion of the middle electrode being disposed contiguous with the silicon-rich insulator,

h) forming a storage-element layer,

i) forming and patterning a second conductive layer over the storage-element layer and disposed to overlay vertically at least a portion of the middle electrode, whereby the second conductive layer is at least partially aligned with the middle electrode, and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell,

j) forming and patterning a second interlayer dielectric, whereby a substrate is formed for subsequent layers,

k) forming vias as required through the second interlayer dielectric, and

l) repeating steps b) through k) until a desired number of memory array layers have been formed.

51. (Withdrawn) The method of claim 50, further comprising the step of patterning the layer of silicon-rich insulator.

52. (Withdrawn) The method of claim 50, further comprising the step of planarizing the first interlayer dielectric.

53. (Withdrawn) The method of claim 50, further comprising the step of planarizing the second interlayer dielectric.

54. (Withdrawn) The method of claim 50, wherein the steps are performed in the order recited.

55. (Previously Presented) A multilayer memory made by a method comprising:

a) providing a substrate,

b) depositing and patterning a first conductive layer over the substrate,

c) forming a tunnel-junction layer over the first conductive layer,

d) forming a layer of silicon-rich insulator over the tunnel-junction layer,

e) forming and patterning a first interlayer dielectric over the layer of silicon-rich insulator,

f) forming an opening through the first interlayer dielectric and extending to the layer of silicon-rich insulator,

g) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode, at least a portion of the middle electrode being disposed contiguous with the silicon-rich insulator,

h) forming a storage-element layer over the patterned first interlayer dielectric,

i) forming and patterning a second conductive layer over the storage-element layer, the patterned second conductive layer being disposed to overlay vertically at least a portion of the middle electrode, whereby a portion of the second conductive layer is aligned with some portion of the middle electrode, and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory cell, and wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected,

j) forming and patterning a second interlayer dielectric over the patterned second conductive layer, whereby a substrate is formed for subsequent layers,

k) forming vias as required through the second interlayer dielectric, and

l) repeating steps b) through k) until a desired number of memory array layers have been formed.

56. (Original) A substrate carrying electronics comprising the multilayer memory of claim 55.

57. (Original) An integrated circuit comprising the multilayer memory of claim 55.

58. (Previously Presented) The memory array of claim 1, wherein the two terminals of the two-terminal memory cell disposed at each cross-point comprise the row conductor and column conductor respectively.

59. (Previously Presented) The memory array of claim 16, wherein the two terminals of the two-terminal memory cell disposed at each cross-point comprise the row conductor and column conductor respectively.

IX. Evidence Appendix

None

X. Related Proceedings Appendix

None

XI. Certificate of Service

None